Fig. 1A

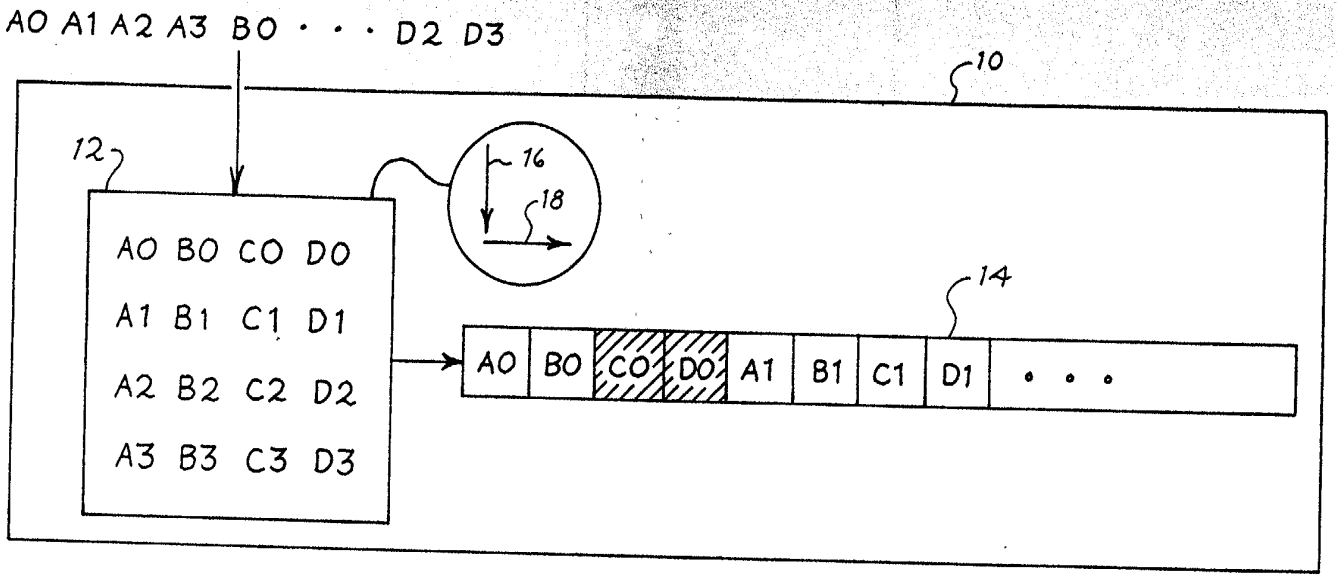
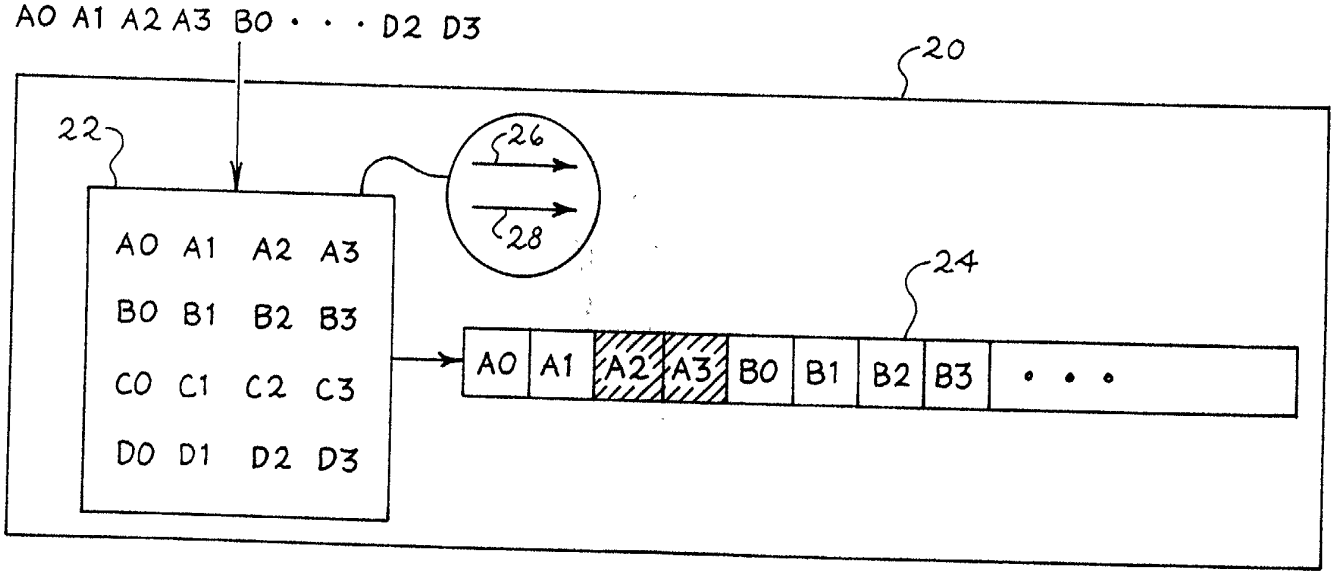

A0 A1 A2 A3 B0 · · · D2 D3
10
12
16
18
A0 B0 C0 D0
A1 B1 C1 D1
A2 B2 C2 D2
A3 B3 C3 D3
14
A0 B0 C0 D0 A1 B1 C1 D1 · · ·

Fig. 1B


A0 A1 A2 A3 B0 · · · D2 D3
20
22
26
28
A0 A1 A2 A3
B0 B1 B2 B3
C0 C1 C2 C3
D0 D1 D2 D3
24
A0 A1 A2 A3 B0 B1 B2 B3 · · ·

20F50 Exhibit

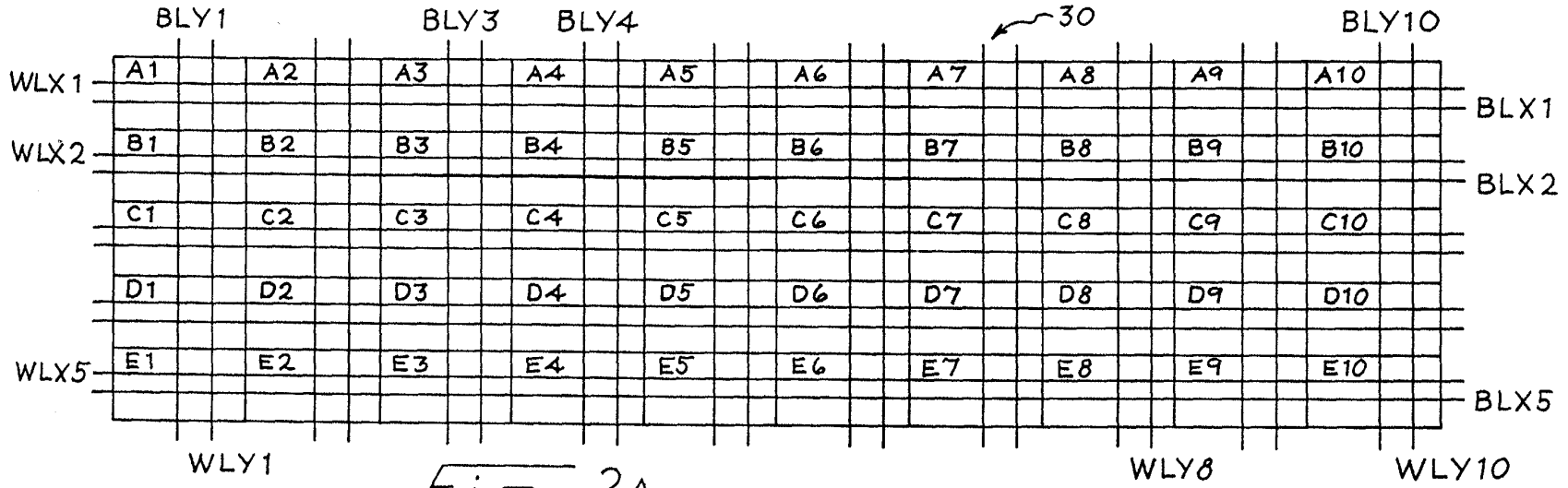


Fig. 2A

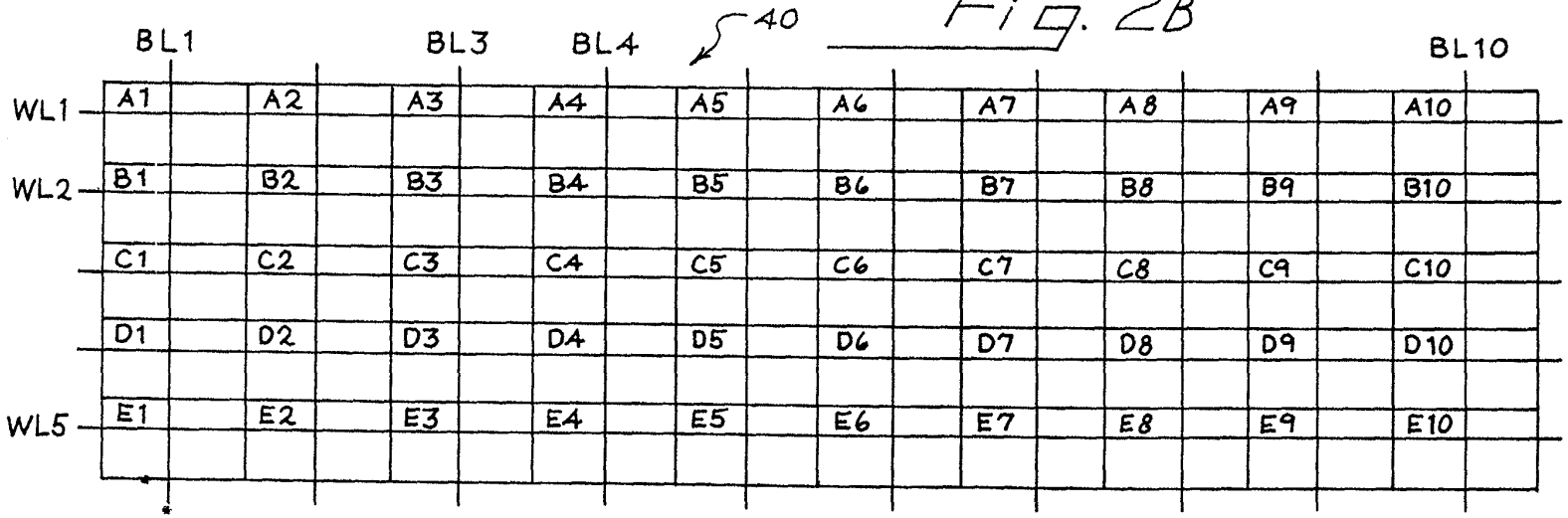


Fig. 2B

Fig. 3

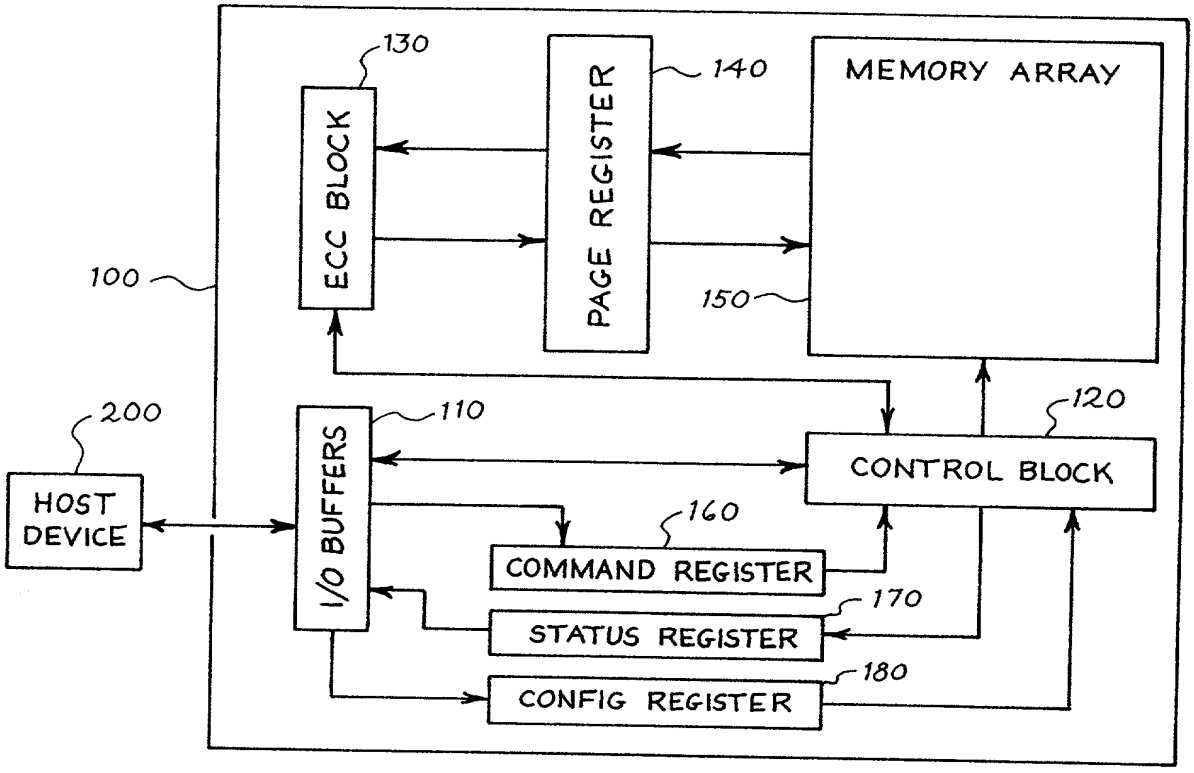
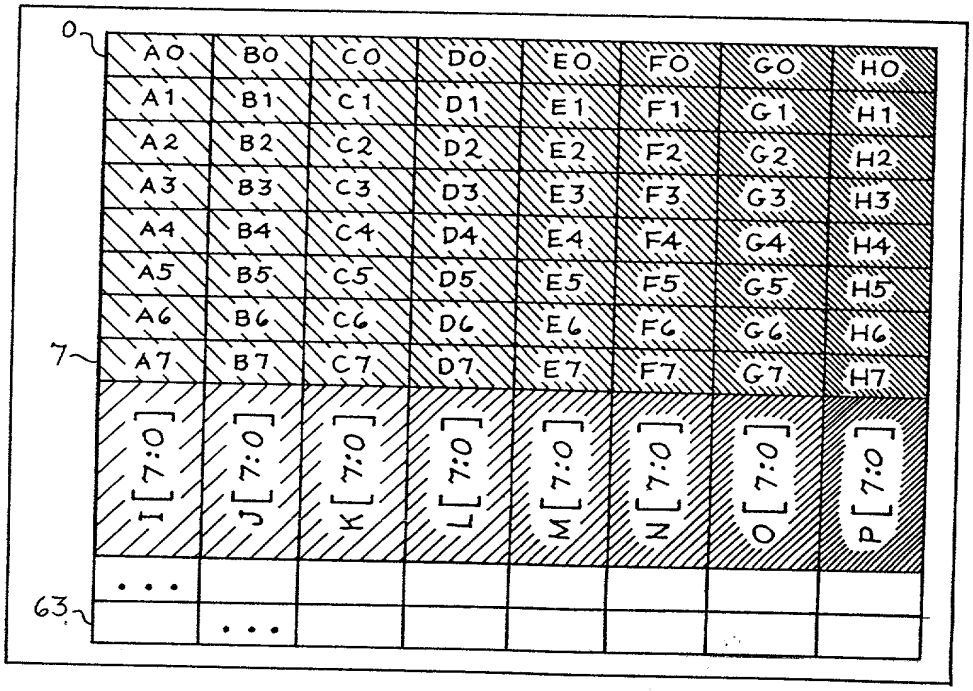

100
130
ECC BLOCK
140
PAGE REGISTER
MEMORY ARRAY
150
200
HOST DEVICE
110
I/O BUFFERS
120
CONTROL BLOCK
160
COMMAND REGISTER
170
STATUS REGISTER
180
CONFIG REGISTER

Fig. 6


0
7
63
A0 B0 C0 D0 E0 F0 G0 H0
A1 B1 C1 D1 E1 F1 G1 H1
A2 B2 C2 D2 E2 F2 G2 H2
A3 B3 C3 D3 E3 F3 G3 H3
A4 B4 C4 D4 E4 F4 G4 H4
A5 B5 C5 D5 E5 F5 G5 H5
A6 B6 C6 D6 E6 F6 G6 H6
A7 B7 C7 D7 E7 F7 G7 H7
I[7:0]
J[7:0]
K[7:0]
L[7:0]
M[7:0]
N[7:0]
O[7:0]
P[7:0]

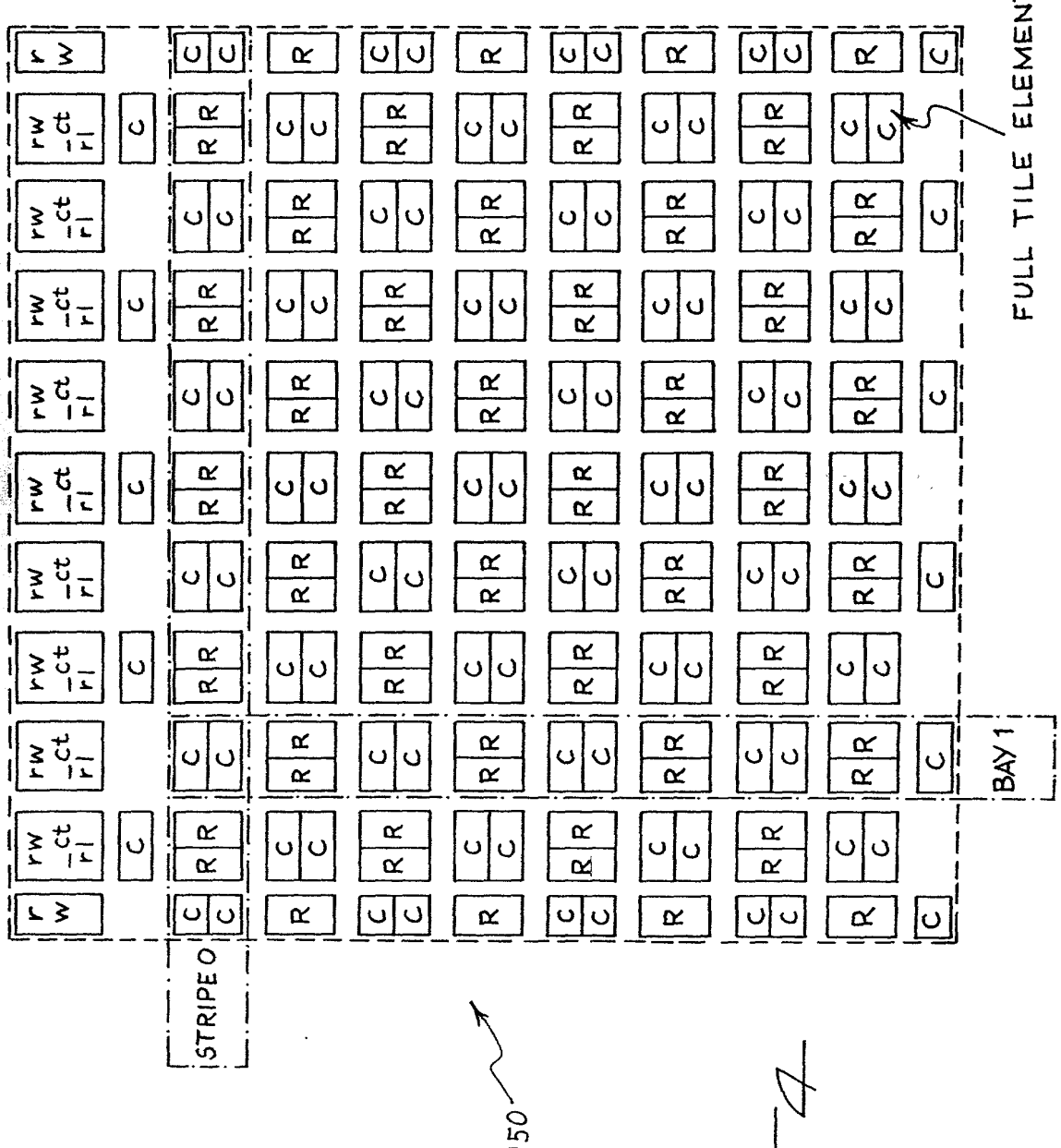


Fig. 4

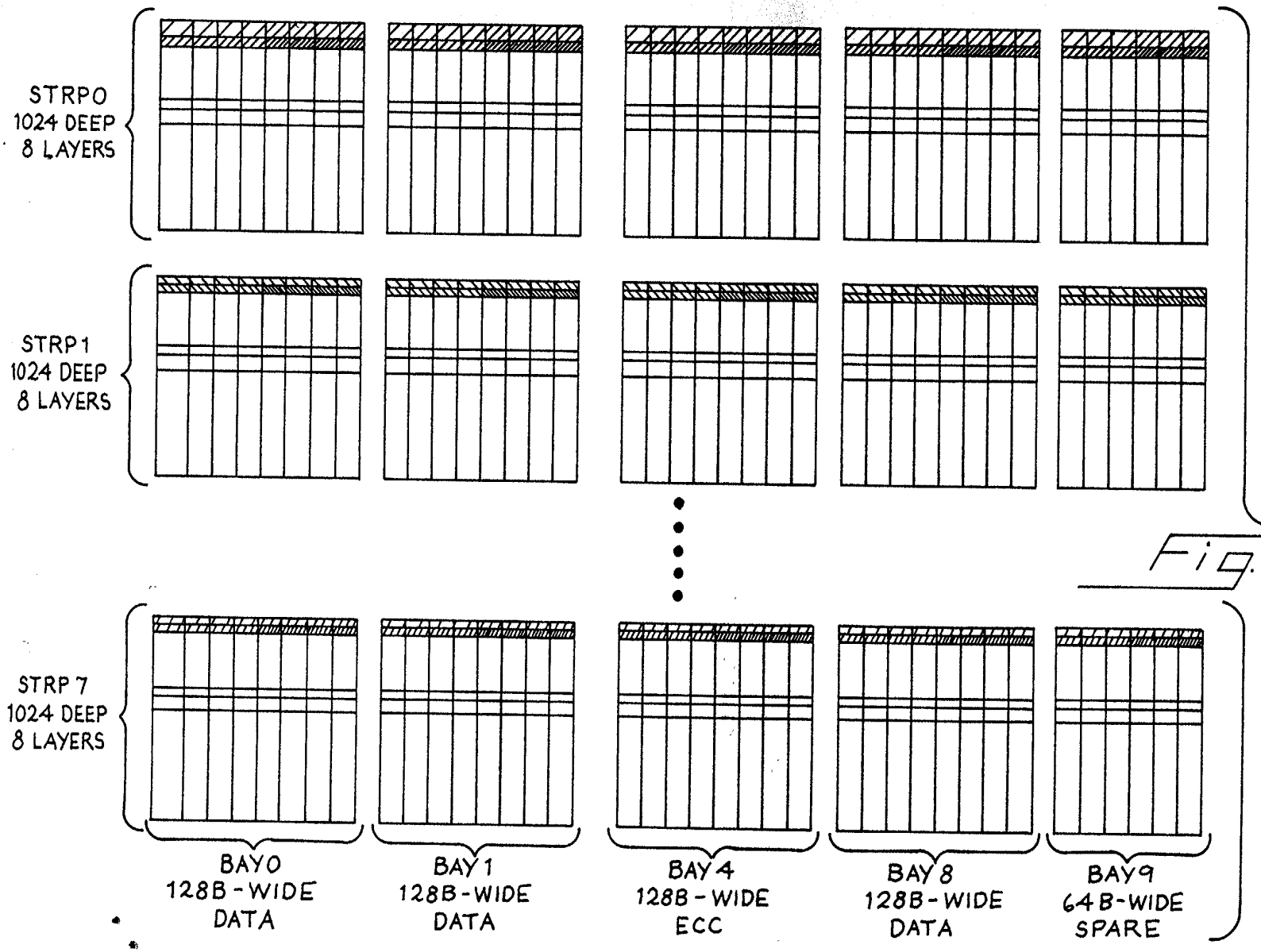

STRP0
1024 DEEP
8 LAYERS
STRP1
1024 DEEP
8 LAYERS
STRP 7
1024 DEEP
8 LAYERS
BAY0
128B-WIDE
DATA
BAY1
128B-WIDE
DATA
BAY4
128B-WIDE
ECC
BAY8
128B-WIDE
DATA
BAY9
64B-WIDE
SPARE

Fig. 5

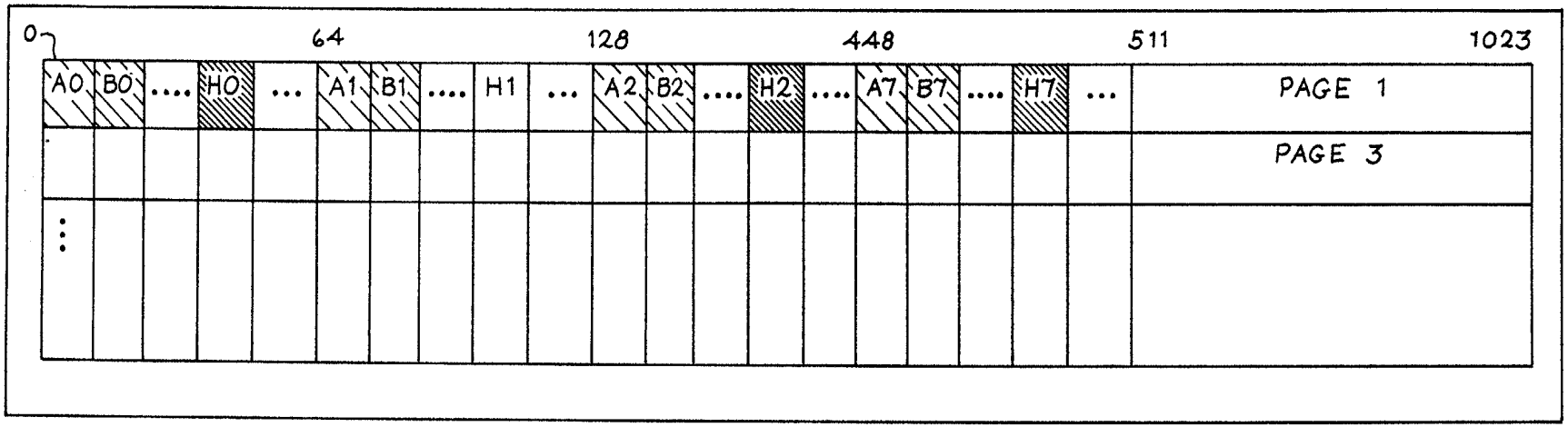

0
64
128
448
511
1023
A0 B0 .... H0 ... A1 B1 .... H1 ... A2 B2 .... H2 .... A7 B7 .... H7 ...
PAGE 1
PAGE 3

Fig. 7

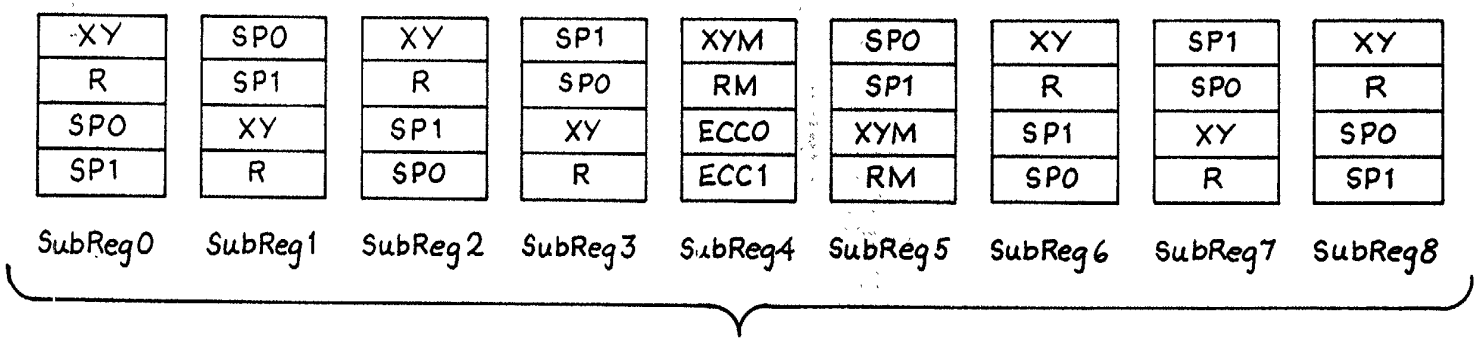

XY R SP0 SP1
SP0 SP1 XY R
XY R SP1 SP0
SP1 SP0 XY R
XYM RM ECC0 ECC1
SP0 SP1 XYM RM
XY R SP1 SP0
SP1 SP0 XY R
XY R SP0 SP1
SubReg0 SubReg1 SubReg2 SubReg3 SubReg4 SubReg5 SubReg6 SubReg7 SubReg8

Fig. 9

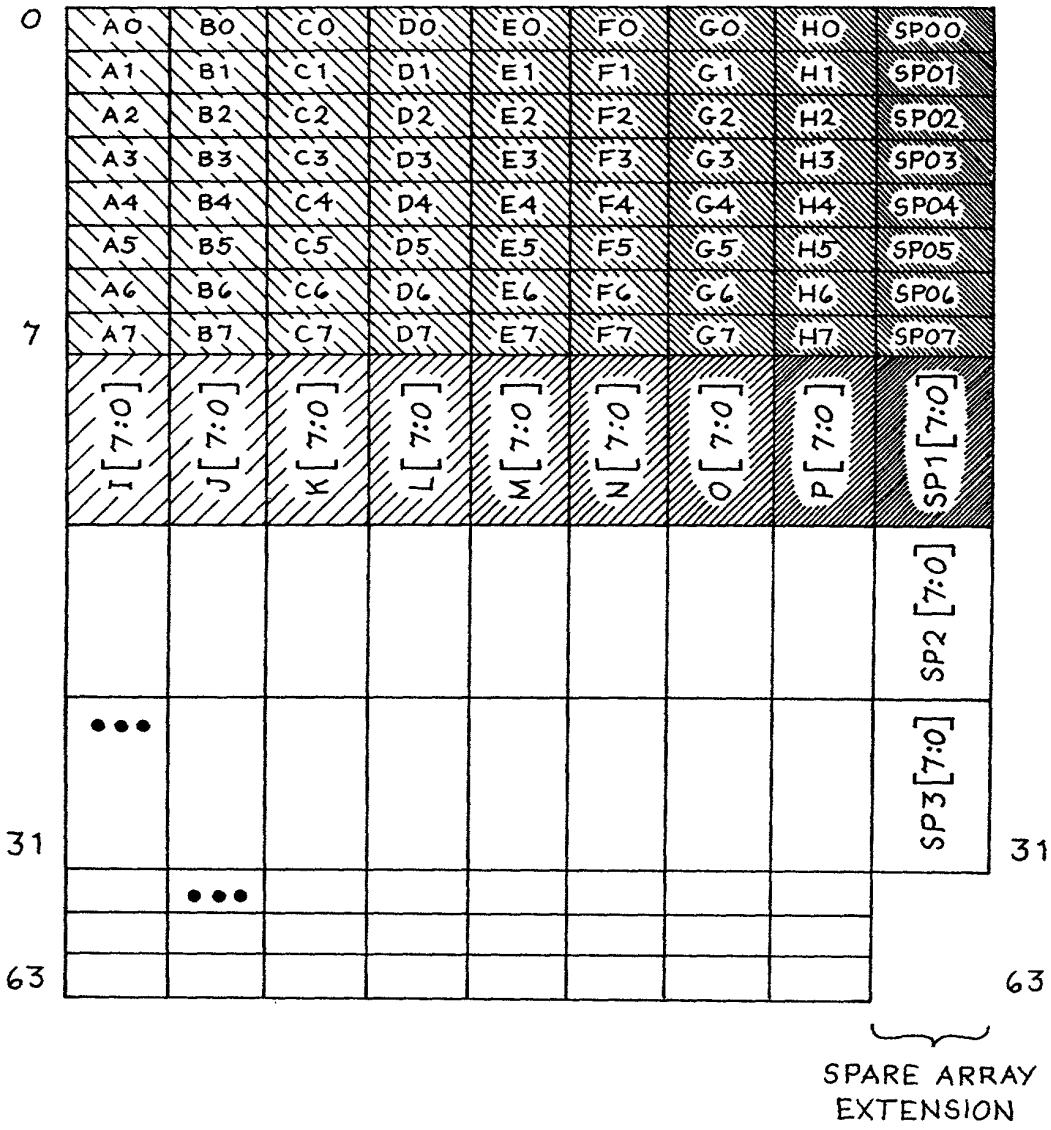

0
7
31
63
A0 B0 C0 D0 E0 F0 G0 H0 SP00
A1 B1 C1 D1 E1 F1 G1 H1 SP01
A2 B2 C2 D2 E2 F2 G2 H2 SP02
A3 B3 C3 D3 E3 F3 G3 H3 SP03
A4 B4 C4 D4 E4 F4 G4 H4 SP04
A5 B5 C5 D5 E5 F5 G5 H5 SP05
A6 B6 C6 D6 E6 F6 G6 H6 SP06
A7 B7 C7 D7 E7 F7 G7 H7 SP07
I [7:0]
J [7:0]
K [7:0]
L [7:0]
M [7:0]
N [7:0]
O [7:0]
P [7:0]
SP1 [7:0]
SP2 [7:0]
SP3 [7:0]
SPARE ARRAY EXTENSION

Fig. 8